

IMPLANTED ASYMMETRIC DOPED POLYSILICON GATE FinFET

Abstract of the Disclosure

An asymmetric field effect transistor (FET) that has a threshold voltage that is compatible with current CMOS circuit designs and a low-resistance gate electrode is provided. Specifically, the asymmetric FET includes a p-type gate portion and an n-type gate portion on a vertical semiconductor body; an interconnect between the p-type gate portion and the n-type gate portion; and a planarizing structure above the interconnect.

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Figure 1 displays a series of 11 line drawings illustrating the progression of a child's drawing of a person from age 2 to age 10. The drawings are arranged vertically, with the youngest at the top and the oldest at the bottom. Each drawing is labeled with its corresponding age: 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, and 12. The drawings show a clear development from simple, abstract shapes to more detailed, human-like figures.